NovoBytes™

Product Brief

A Microchip Technology Company

NovoBytes – Addressable Array
256 – 32Kbits OTP Antifuse Memory

This document provides abbreviated datasheet information for NovoBytes memory IP. It outlines the general OTP functionality for the SST IP and provides an introduction to the performance and functionality for the products. The full IP datasheet is available under confidentiality agreement terms, and includes customer specific requirements as well as additional information relevant to the integration of all NovoBytes memory IP blocks into IC design projects.

General Description

SST's core technology is utilized throughout the Smartbit™-based product family including the NovoBytes product line. All peripheral circuits are operated within process specifications and the breakdown voltage is confined entirely within the memory core. Unprogrammed cells are never subjected to voltages outside of native process parameters and have the same reliability as the underlying CMOS technology. SST's Smartbit™ bit cell uses a patented oxide-breakdown antifuse technology that is designed to maximize both device reliability and programming yield while offering faster programming than other OTP technologies. The write protocol with active sensing ensures hard breakdown of the gate oxide and the creation of a permanent short between the gate polysilicon and the channel of a programmed device. As the program time varies from cell to cell, this programming method eliminates the effect of having some cells not programmed as strongly as other cells which is typical of other solutions. It also avoids the data retention issues of floating gate designs.

Functional Description

The NovoBytes One-Time-Programmable (OTP) non-volatile memory block is organized as a ROM architecture with separate data inputs/outputs. The memory is programmed one word at a time with only bits set to a logic "1" being programmed. Each bit supports infinite reads and one write

About Silicon Storage Technology, Inc.

SST is the creator of SuperFlash®, an innovative, highly reliable and versatile type of NOR Flash memory. SST, the leader in embedded flash memory, was founded in 1989, and went public in 1995. SST was acquired by Microchip Technology, Inc. in April 2010, and now it is a wholly own subsidiary of Microchip Technology, Inc. SST focuses on licensing embedded NVM technology to Foundries, IDMs and Fabless companies. In June of 2013, SST completed the acquisition of Novocell Semiconductor, developers of an innovative Smartbit™ antifuse one-time programmable (OTP) NVM. Founded in 2001, Novocell Semiconduc¬tor, Inc. specialized in developing and delivering advanced, high reliability non-volatile memory IP to the semiconductor industry. The dedicated design team has extensive experience in custom memory IP development

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Features

- **Implemented in standard logic CMOS with no additional process steps or post processing**
- **Reliable antifuse technology**
- **Breakdown voltage contained entirely in the memory core**
- **Maintained Parallel Outputs**
- **In-circuit programmable**
- **> 30 years retention**
- **Low programming current**
- **4 metal layers used**
- **Allows routing over macro**
- **Compact size**
- **-40°C to +125°C operating temperature**

Overview

NovoBytes is part of the Smartbit™-based family of One-Time-Programmable (OTP) non-volatile memory blocks that can be embedded in standard logic CMOS with no additional process steps or post processing. It is based upon a patented, reliable, well understood antifuse mechanism that has been silicon proven in a wide range of CMOS technologies.

Programming requires no additional external hardware, and programming voltages are generated entirely within the memory core. Self-contained control logic handles all programming sequencing and verification.

Architecture

The NovoBytes memory requires two voltage supplies (VDD & VPGM). VDD is the core and logic voltage supply used when the memory is being read or written. VPGM is the programming voltage.

Programming the memory is performed by setting the input data and address bits and completing a write cycle. Each bit is programmed until a hard breakdown occurs, the duration of which will vary from cell to cell Once programming is complete, the DONE pin will be asserted. The user must monitor the DONE pin to end the write cycle. Unprogrammed bits are zeros and programmed bits are ones.
After a reset, it is required to wait for the sensing circuit to settle before reading the memory.